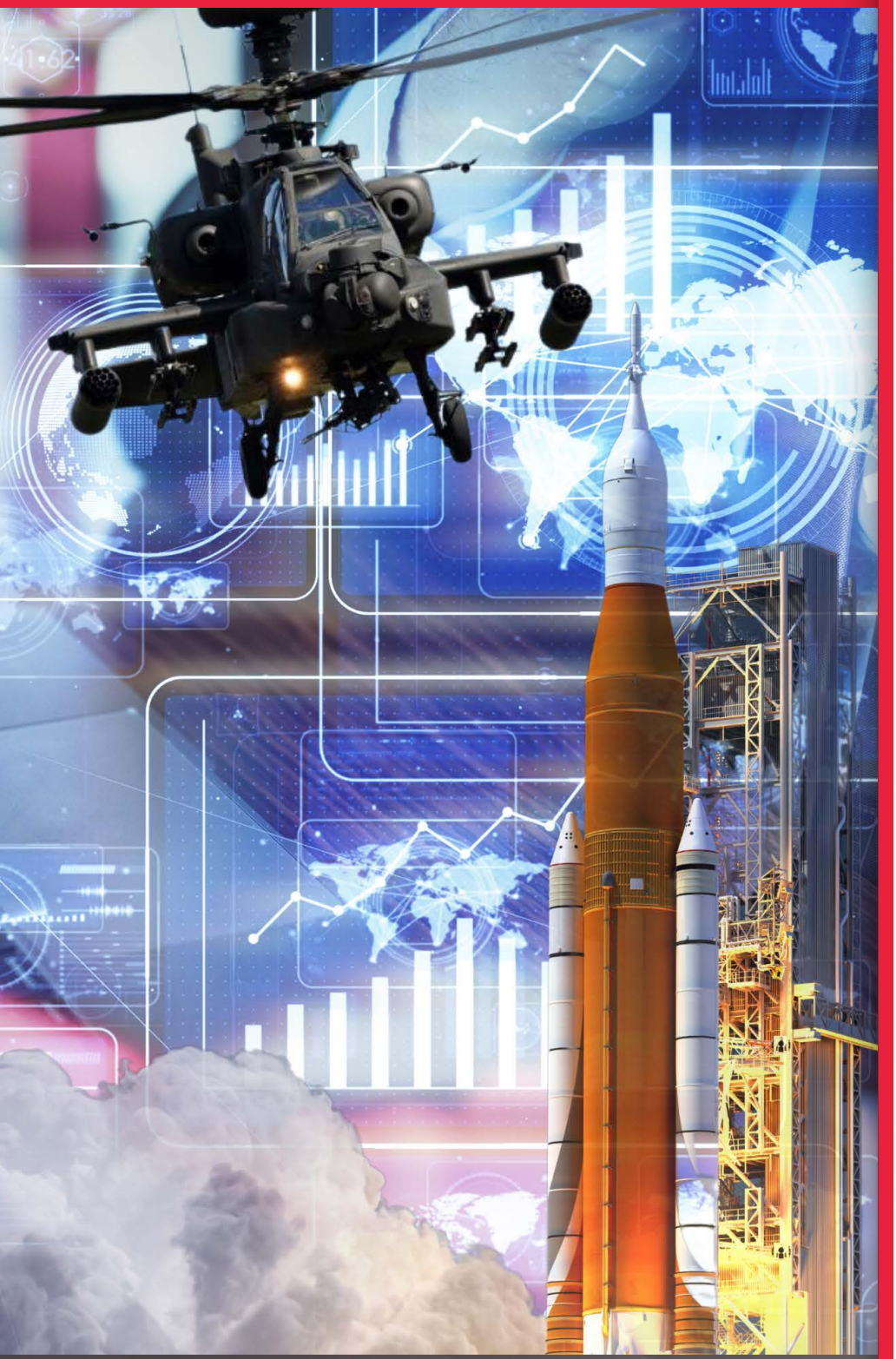
Software Life Cycle Management



TriVector's recognized software experts provide superior *value* to our customers through their wide ranging software *experience* and proven *performance*.

- *Software Development Planning and Management*
- *Software Analysis, Safety, and Airworthiness*
- *Software Test and Evaluation - Development through Qualification*
- *Software Lab Management and Execution*
  - *AH-64 Apache Post Production Software Support Lab*
  - *Model-Based Systems Engineering (MBSE) Software Development*

Certiÿcations and Standards

- *RTCA DO-178C Compliance Analysis and Lifecycle Management*
- *IEEE 12207*
- *Software Engineering Evaluation System (SEES) Procedures and Deliverables Update and Working Group Member*

Our People

- *99% Employee Satisfaction*
- *95% Employee Retention*
- *51% Advanced Degrees*
- *32% Subject Matter Experts*

Our Current Customers

- *U.S. ARMY: CCDC AvMC*
- *Missile Defense Agency (MDA)*
- *NASA: Space Launch* System (SLS)

Experience ▸ Performance ▸ Value

TriVector SERVICES INC.

Delivering Innovative Software Solutions...Achieving Optimal System Performance

S3I Software Mission Assurance

TriVector actively supports tasks for UH-60V, UH-60, MH-47G-MG-60M, and Multisystem Software Airworthiness (SW/AW) Support. With so many platforms to support, our team performs a wide array of tasks. Our team has initiated the development of software reuse airworthiness requirements to support the qualification of IME software and develops software lifecycle data items to reflect active version status as well as functional updates. In Ground Based Sense and Avoid (GBSAA), we are currently supporting six Block 1 fielded systems and site design is ongoing for four additional fielding locations. We work closely with the UH-60 S3I team performing review and audit of SW/AW lifecycle data items and artifacts and are currently developing the memory adversarial application necessary for performing airworthiness evaluation of UH60V and replicating the corresponding data they generate for memory.

AH-64 Apache Post Production Software Support (PPSS) Lab Team

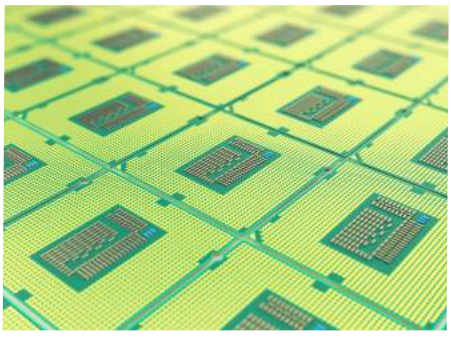
The AH-64 Apache PPSS Lab Team is in the process of establishing a capability to modify, build, integrate, and test tactical software changes for fielded Apache Block II aircraft system software. TriVector developed a consolidated bi-directional Requirements Verification Traceability Matrix (RVTM) based on several disparate source documents, including the Software Requirements Specifications, Design Documents, Test Plans, Test Descriptions, and Test Reports. This RVTM has been instrumental in the tracking of changes to the software baseline and in the identification of regression test cases and scripts for Apache PPSS software builds.

NASA Space Launch System (SLS) Avionics Software Timing

NASA's SLS is an advanced launch vehicle for a new era of exploration beyond Earth's orbit. It integrates new technologies with heritage components to process critical commands, measurements, and less critical data. The integration of heritage avionics subsystems presented unique challenges for time correlation across the vehicle. TriVector engineers developed stringent but realistic timing requirements, detailed verification objectives, and analysis approaches for SLS flight software, subsystem firmware, and the test environment. TriVector led the early development of test procedures to accelerate testing, develop compli-ance data, characterize time errors, and increase confidence in flight readiness.

AH-64 Apache Version 6 Multi-Core Processor (MCP) Software Airworthiness

AH-64 Apache Version 4.5/6 aircraft are complex rotary wing systems with MCP software architecture. The MCP architecture presented challenges to airworthiness qualification related determinations due to its process partitioning and shared resources. TriVector assessed and provided recommendations for MCP architecture implementation, without an ARINC-653 RTOS, to achieve CAST-32A Multi-core Processors policy implementation compliance. We assisted the Aviation Engineering Directorate and the Apache PM in defining the airworthiness position to ensure substantiation for compliance with CAST-32A. This was achieved by confirming single cores containing safety critical functions have no overruns and that safe worst case execution times are sufficient.



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